

FIG. 1

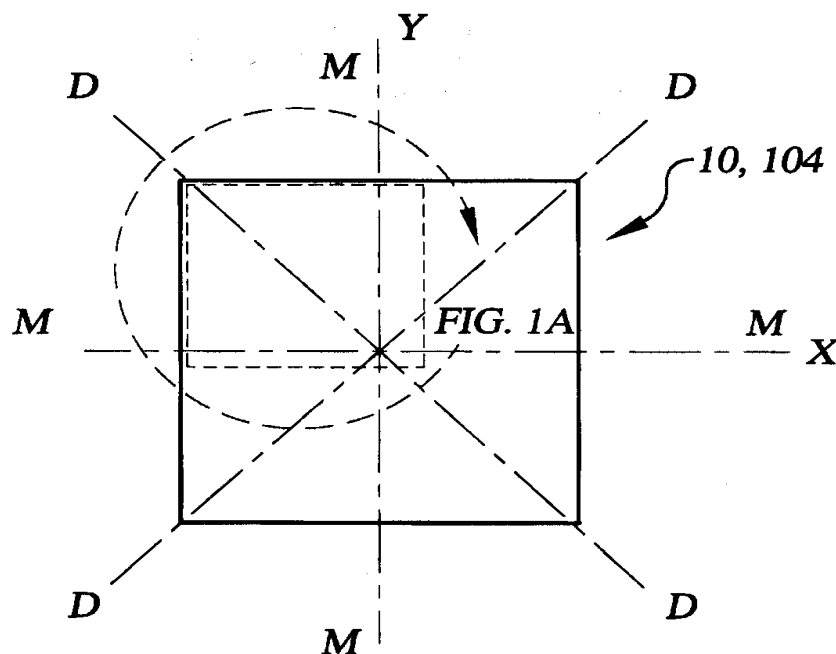


FIG. 1A

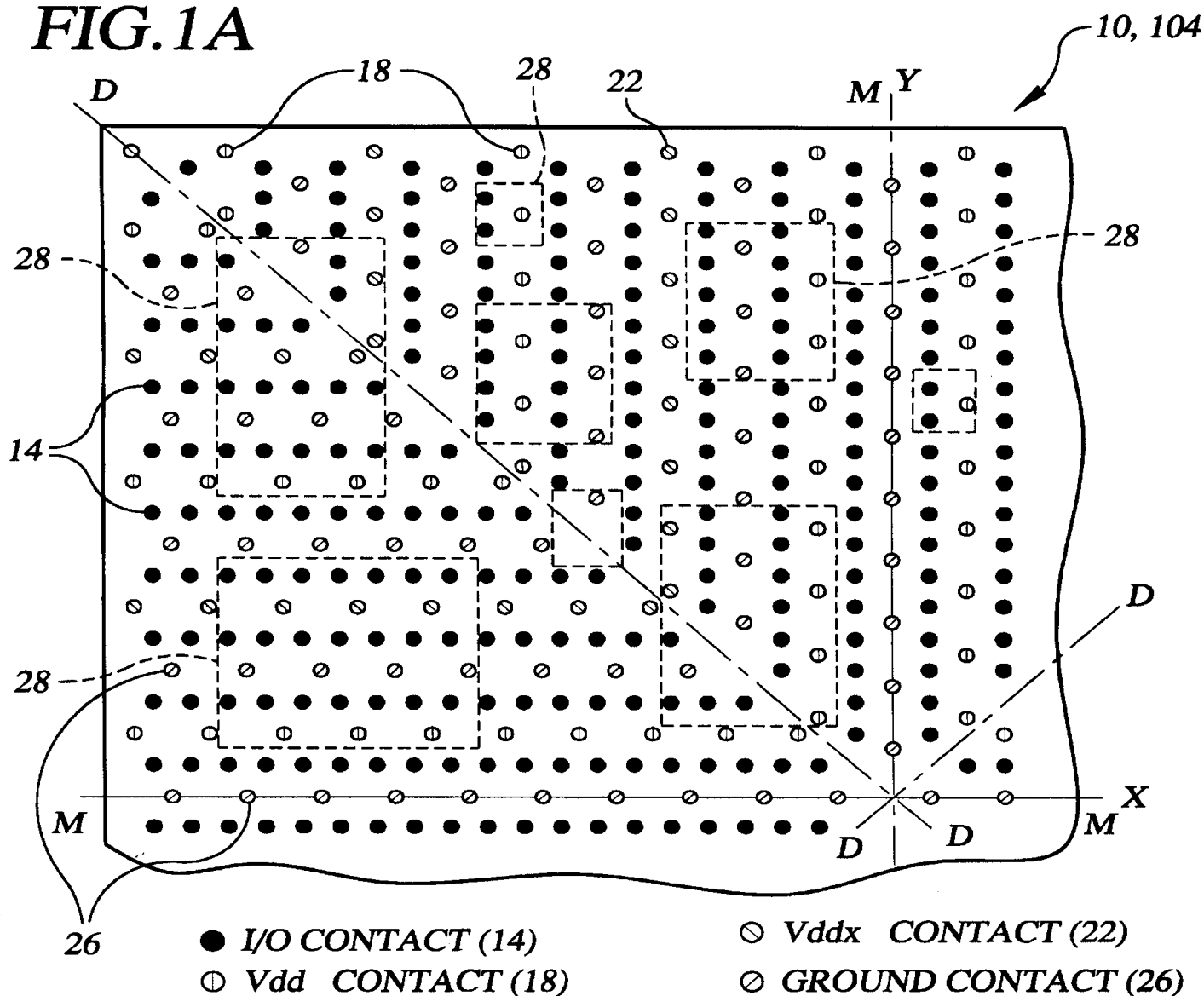


FIG.2
PRIOR ART

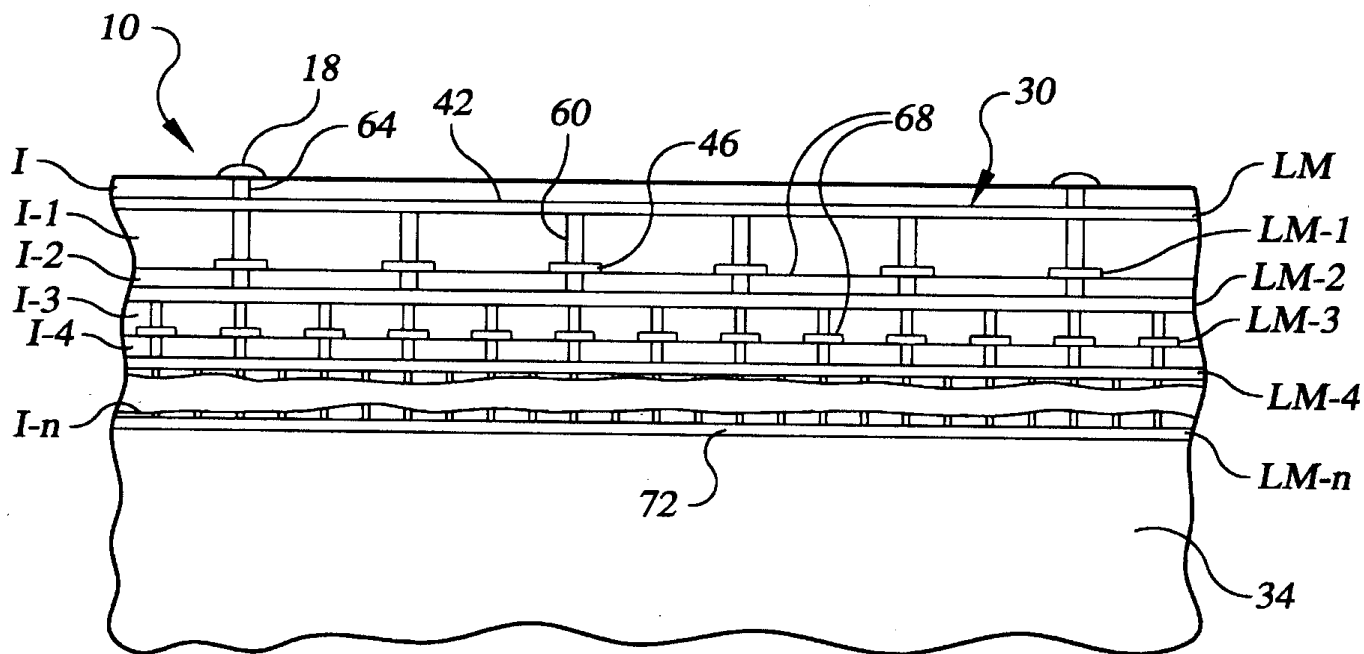
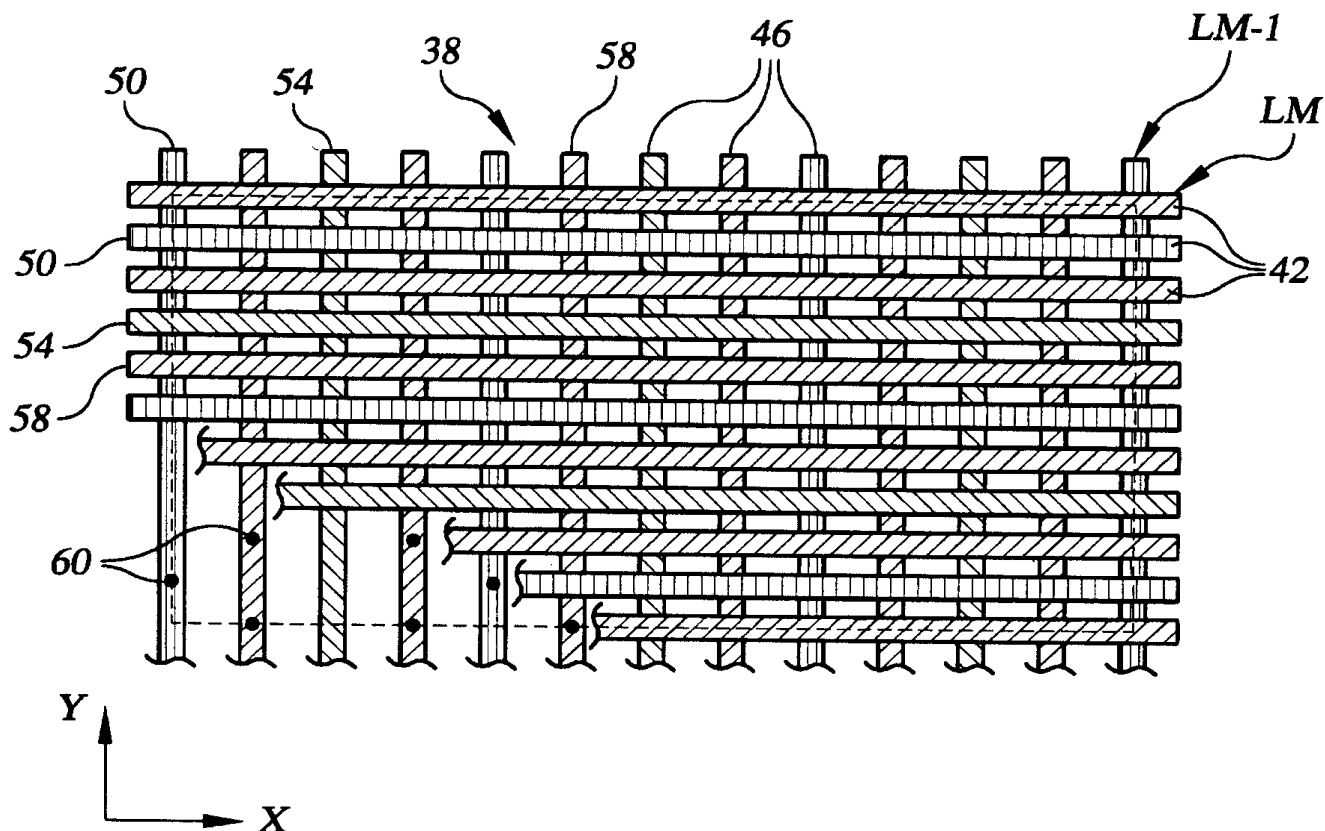
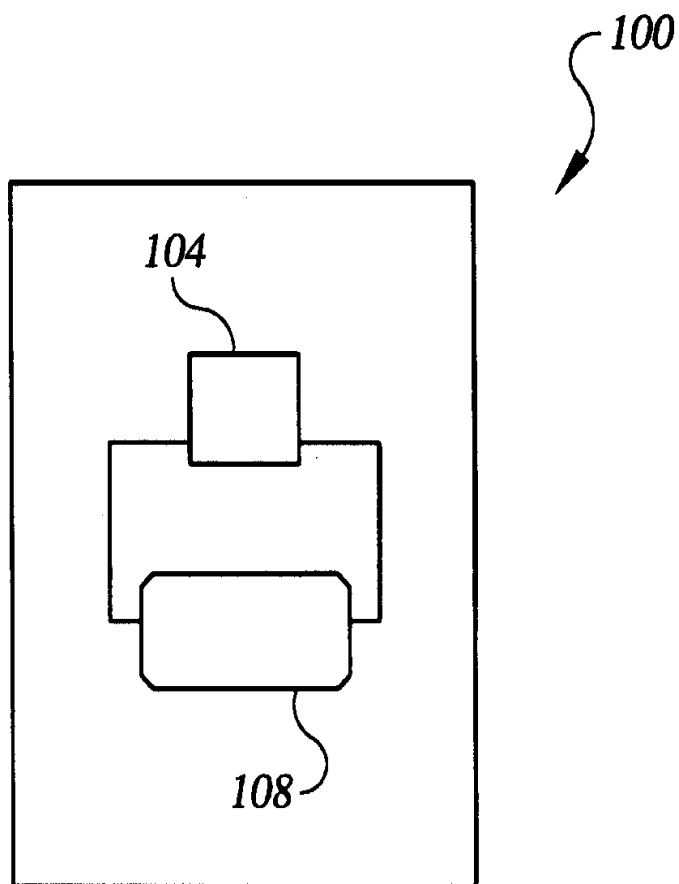


FIG.3
PRIOR ART



INTEGRATED CIRCUIT CHIP HAVING A RINGED WIRING LAYER
INTERPOSED BETWEEN A CONTACT LAYER AND A WIRING GRID
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FIG.4



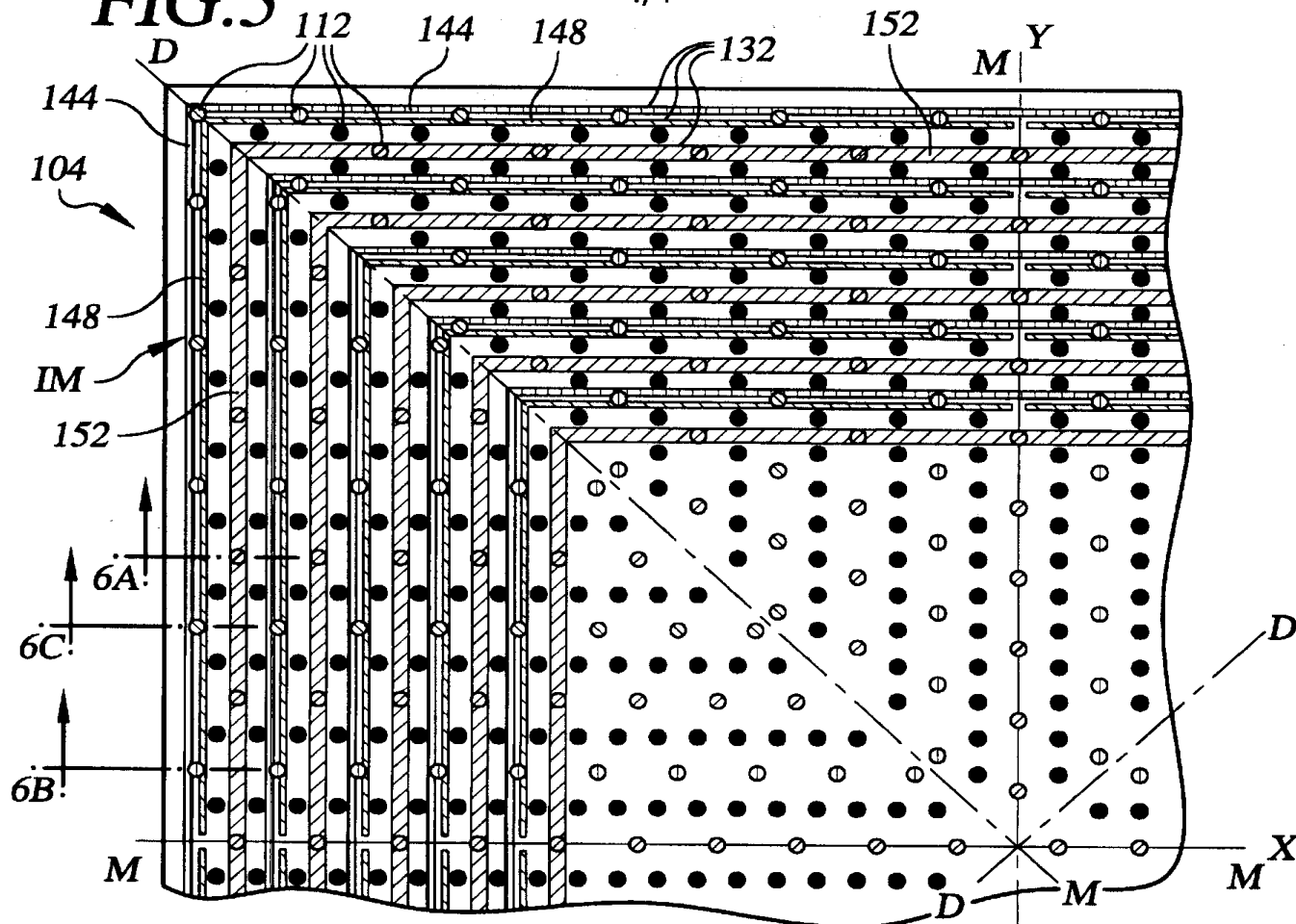
INTEGRATED CIRCUIT CHIP HAVING A RINGED WIRING LAYER INTERPOSED BETWEEN A CONTACT LAYER AND A WIRING GRID

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FIG. 5



○ Vdd CONTACT (116)

○ Vddx CONTACT (120)

○ GROUND CONTACT (124)

● I/O CONTACT (128)

FIG. 6A

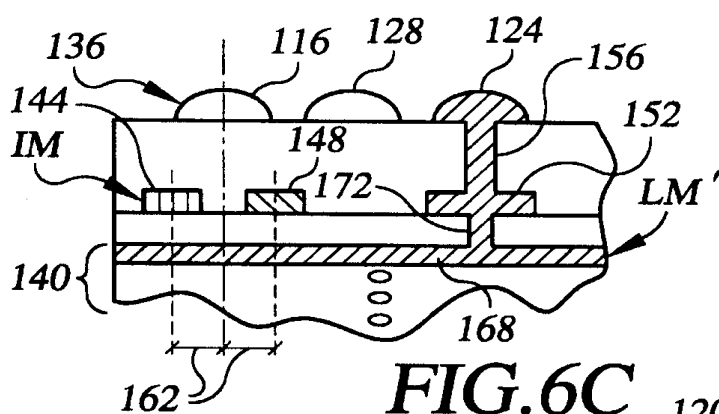


FIG. 6B

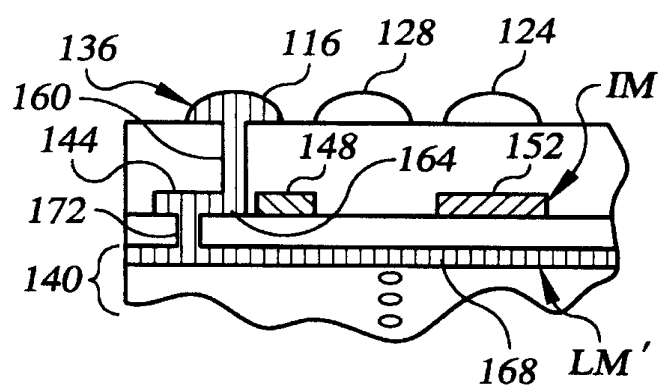


FIG. 6C

